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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/610,753	07/06/2000	Shunpel Yamazaki	SEL 195	5666

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EXAMINER	
BROCK II, PAUL E	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/610,753	YAMAZAKI ET AL.
	Examiner	Art Unit
	Paul E Brock II	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) *2,4-20,22,24,26 and 28-52* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,21,23,25,27 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *16* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 2, 4 – 20, 22, 24, 26 and 28 – 52 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the p-channel TFT of the driver circuit not having an LDD region must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it

> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 3, 21, 23, 25, 27, and 53 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification support for "wherein the p-channel TFT of the driver circuit does not have a LDD region," can be found.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto (USPAT 5323042, Matsumoto) in view of Shimone (JPPAT 6258659) and Adan et al. (USPAT 5841170, Adan).

With regard to claim 1, Matsumoto discloses in figure 1 a semiconductor device. Matsumoto discloses in figure 1 a pixel TFT (21) disposed in a pixel section over a substrate (11), and a driver circuit comprising a p-channel TFT (23) and an n-channel TFT (22), over the substrate. Matsumoto discloses in figure 1 a second interlayer insulating film (29) over a gate electrode (27) of the pixel TFT. Matsumoto does not disclose a first interlayer insulating film

comprising an inorganic insulator or that the second interlayer insulating film comprises an organic insulating material. Shimone discloses in figure 3d a first interlayer insulating film (113) comprising an inorganic insulating material over a gate electrode (106) of a pixel TFT. Shimone discloses in figure 3d a second interlayer insulating film (104) comprising an organic insulating material over the first interlayer insulating film. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the organic insulating layer and inorganic insulating film of Shimone in the device of Matsumoto in order to use a material capable of photo imaging as the interlayer dielectric. Matsumoto discloses in figure 1 a pixel electrode (32) having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an opening in the second interlayer insulating film. Shimone further teaches a pixel electrode (106) having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an opening in the first and second interlayer insulating films. Therefore it would have been further obvious to one of ordinary skill in the art at the time of the present invention that the opening of Matsumoto and Shimone would be in the first and second insulating layers. Matsumoto discloses in figure 1 wherein the p-channel TFT of the driver circuit comprises a channel forming region (23a) a source region (right, 23b and 23c) and a drain region (left, 23b and 23c) in contact with the channel forming region. As far as the examiner can ascertain, the p-channel TFT of the driver circuit does not have a LDD region. Matsumoto discloses in figure 1 wherein the n-channel TFT of the driver circuit comprises a channel forming region (22a), an n-type impurity region of a first concentration (22b) which forms at least one LDD region in contact with the channel forming region, and a source region and a drain region in contact with the at

least one LDD region. Matsumoto and Shimone not disclose that the LDD region is partly overlapping a gate electrode (26). Adan teaches in figure 29; column 2, lines 17 – 25; column 11, lines 58 – 60; column 12, lines 9 – 11; and column 13, lines 49 – 51 wherein an n-channel TFT (61a) of the driver circuit comprises a channel forming region (65), an n-type impurity region of a first concentration which forms at least one LDD region (71) in contact with the channel forming region and partly overlapping a gate electrode (66), and a source region (63) and a drain region (64) in contact with the at least one LDD region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the partly overlapping LDD regions of Adan in the device of Matsumoto and Shimone in order to increase the breakdown voltage of the transistor as stated by Adan in column 2, lines 17 – 25.

Matsumoto discloses in figure 1 wherein the pixel TFT comprises a channel forming region (21a), at least one LDD region (21b) in contact with the channel forming region, and a source region (left 21c) and a drain region (right (21c) in contact with the at least one LDD region.

With regard to claim 25, the semiconductor device of Matsumoto, Adan and Shimone could obviously be part of a personal computer.

7. Claims 3 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Shimone, Karauchi et al. (JPPAT 9120072, Karauchi) and Adan.

With regard to claim 3. Matsumoto discloses in figure 1 a semiconductor device. Matsumoto discloses in figure 1 a pixel TFT (21) disposed in a pixel section over a first substrate (11). Matsumoto discloses in figure 1 a driver circuit comprising a p-channel TFT (23) and an n-

channel TFT (22), over the first substrate. Matsumoto discloses in figure 1 a second interlayer insulating film (29) over a gate electrode (27) of the pixel TFT. Matsumoto does not disclose a first interlayer insulating film comprising an inorganic insulator or that the second interlayer insulating film comprises an organic insulating material. Shimone discloses in figure 3d a first interlayer insulating film (113) comprising an inorganic insulating material over a gate electrode (106) of a pixel TFT. Shimone discloses in figure 3d a second interlayer insulating film (104) comprising an organic insulating material over the first interlayer insulating film. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the organic insulating layer and inorganic insulating film of Shimone in the device of Matsumoto in order to use a material capable of photo imaging as the interlayer dielectric. Matsumoto discloses in figure 1 a pixel electrode (32) having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an opening in the second interlayer insulating film. Shimone further teaches a pixel electrode (106) having a light reflective surface over the second interlayer insulating film, and is electrically connected with the pixel TFT through an opening in the first and second interlayer insulating films. Therefore it would have been further obvious to one of ordinary skill in the art at the time of the present invention that the opening of Matsumoto and Shimone would be in the first and second insulating layers. Matsumoto and Shimone do not disclose a columnar spacer, a second substrate, or a liquid crystal. Karauchi discloses in figure 7 at least a columnar spacer covering an opening. Karauchi discloses in figure 7 a second substrate (111) having a transparent conductive film stuck to the first substrate through the at least one columnar spacer. Karauchi discloses in figure 7 a liquid crystal sandwiched between the first and second substrates. It would have been

obvious to one of ordinary skill in the art at the time of the present invention to use the columnar spacer, second substrate, and liquid crystal of Karauchi in the device of Matsumoto, Shimone in order to create a liquid crystal display with constant distance between substrates. Matsumoto discloses in figure 1 wherein the p-channel TFT of the driver circuit comprises a channel forming region (23a), a source region (right, 23b and 23c), and a drain region (left, 23b and 23c) in contact with the channel forming region. As far as the examiner can ascertain, the p-channel TFT of the driver circuit does not have a LDD region. Matsumoto discloses in figure 1 wherein the n-channel TFT of the driver circuit comprises a channel forming region (22a), an n-type impurity region of a first concentration (22b) which forms at least one LDD region in contact with the channel forming region, and a source region, and a drain region in contact with the at least one LDD region. Matsumoto, Shimone and Karauchi not disclose that the LDD region is partly overlapping a gate electrode (26). Adan teaches in figure 29; column 2, lines 17 – 25; column 11, lines 58 – 60; column 12, lines 9 – 11; and column 13, lines 49 – 51 wherein an n-channel TFT (61a) of the driver circuit comprises a channel forming region (65), an n-type impurity region of a first concentration which forms at least one LDD region (71) in contact with the channel forming region and partly overlapping a gate electrode (66), and a source region (63) and a drain region (64) in contact with the at least one LDD region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the partly overlapping LDD regions of Adan in the device of Matsumoto, Shimone and Karauchi in order to increase the breakdown voltage of the transistor as stated by Adan in column 2, lines 17 – 25. Matsumoto discloses in figure 1 wherein the pixel TFT comprises a channel forming region (21a), at least

one LDD region (21b) in contact with the channel forming region, and a source region (21c) and a drain region (21c) in contact with the at least one LDD region.

With regard to claim 27, the semiconductor device of Matsumoto, Adan and Shimone could obviously be part of a personal computer.

8. Claims 21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto, Shimone, Karauchi, and Adan as applied to claim 3 above, and further in view of Hioki (JPPAT 8234212).

With regard to claim 21, Matsumoto, Shimone, Karauchi, and Adan do not disclose a columnar spacer over the TFTs of the driver circuit. Hioki discloses in figure 1 a columnar spacer (24) formed over TFTs (22) of the driver circuit. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the columnar spacer of Hioki to cover the p-channel TFT and the n-channel TFT in the device of Matsumoto, Shimone, Karauchi, and Adan in order to eliminate forming spacers on pixel electrodes as stated by Hioki.

With regard to claim 22, Matsumoto, Shimone, Karauchi, and Adan do not disclose a columnar spacer formed to cover at least a source wiring of the p-channel TFT and the n-channel TFT. Hioki discloses in figure 1 a columnar spacer formed to cover source wirings of TFTs. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the columnar spacer of Hioki to cover the source wirings of the p-channel TFT and the n-channel TFT in Matsumoto, Shimone, Karauchi, and Adan in order to eliminate forming spacers on pixel electrodes as stated by Hioki.

9. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Shimone, Takasu (USPAT 5982002, Takasu), and Adan.

With regard to claim 3, Matsumoto discloses in figure 1 a semiconductor device. Matsumoto discloses in figure 1 a pixel TFT (21) having disposed in a pixel section over a substrate (11). Matsumoto discloses in figure 1 a driver circuit comprising a p-channel TFT (23) and an n-channel TFT (22), over the substrate. Matsumoto discloses in figure 1 a second interlayer insulating film (29) over a gate electrode (27) of the pixel TFT. Matsumoto does not disclose a first interlayer insulating film comprising an inorganic insulator or that the second interlayer insulating film comprises an organic insulating material. Shimone discloses in figure 3d a first interlayer insulating film (113) comprising an inorganic insulating material formed over of a pixel section. Shimone discloses in figure 3d a second interlayer insulating film (104) comprising an organic insulating material over the first interlayer insulating film. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the organic insulating layer and inorganic insulating film of Shimone in the device of Matsumoto in order to use a material capable of photo imaging as the interlayer dielectric. Matsumoto discloses in figure 1 a pixel electrode (32) having a light reflective surface over the second interlayer insulating film, and in connected to the pixel TFT through an opening in the second interlayer insulating film. Shimone further teaches a pixel electrode (106) having a light reflective surface over the second interlayer insulating film, and in connected to the pixel TFT through an opening in the first and second interlayer insulating films. Therefore it would have been further obvious to one of ordinary skill in the art at the time of the present invention that the opening of Matsumoto and Shimone would be in the first and second insulating layers. Matsumoto discloses

in figure 1 a source wiring (31) over the interlayer insulating film. Matsumoto and Shimone do not teach an alignment film and liquid crystal over the pixel electrode and the source wiring. Takasu teaches in figure 1 an alignment film (114) over a pixel electrode (111) and a source wiring (112). Takasu teaches in figure 1 a liquid crystal sandwiched between the alignment film and an opposed substrate (115). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the alignment film and liquid crystal of Takasu in the device of Matsumoto and Shimone for aligning the orientation of liquid crystal molecules as stated by Takasu in column 7, lines 28 – 33. Matsumoto discloses in figure 1 wherein the p-channel TFT of the driver circuit comprises a channel forming region (23a), a source region (right, 23b and 23c), and a drain region (left, 23b and 23c) in contact with the channel forming region. As far as the examiner can ascertain, the p-channel TFT of the driver circuit does not have a LDD region. Matsumoto discloses in figure 1 wherein the n-channel TFT of the driver circuit comprises a channel forming region (22a), an n-type impurity region of a first concentration (22b) which forms at least one LDD region in contact with the channel forming region, and a source region, and a drain region in contact with the at least one LDD region. Matsumoto, Shimone and Takasu not disclose that the LDD region is partly overlapping a gate electrode (26). Adan teaches in figure 29; column 2, lines 17 – 25; column 11, lines 58 – 60; column 12, lines 9 – 11; and column 13, lines 49 – 51 wherein an n-channel TFT (61a) of the driver circuit comprises a channel forming region (65), an n-type impurity region of a first concentration which forms at least one LDD region (71) in contact with the channel forming region and partly overlapping a gate electrode (66), and a source region (63) and a drain region (64) in contact with the at least one LDD region. It would have been obvious to one of ordinary

skill in the art at the time of the present invention to use the partly overlapping LDD regions of Adan in the device of Matsumoto, Shimone and Takasu in order to increase the breakdown voltage of the transistor as stated by Adan in column 2, lines 17 – 25. Matsumoto discloses in figure 1 wherein the pixel TFT comprises a channel forming region (21a), at least one LDD region (21b) in contact with the channel forming region, and a source region (21c) and a drain region (21c) in contact with the at least one LDD region. Matsumoto discloses in figure 1 wherein the pixel electrode and the source wiring are formed, simultaneously.

Response to Arguments

10. Applicant's arguments filed December 16, 2002 have been fully considered but they are not persuasive.

11. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
March 4, 2003

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